WHAT IS CLAIMED IS:

1.(Amended) A copper alloy for wiring composed of a polycrystalline copper alloy containing Cu (copper) as a primary element and an additional element, wherein

concentration of the additional element is, at grain boundaries of crystal grains composing the polycrystalline copper alloy and in vicinities of grain boundaries, higher than that of the inside of the crystal grains, and

the oxide of the additional element are formed at said grain boundaries and/or in vicinities of said grain boundaries.

2.(Amended) The copper alloy for wiring as set forth in Claim 1 or 5, wherein

the additional element is at least one element selected from a group consisting of Ti (titanium), Zr (zirconium), Hf (hafnium), Cr (chromium), Co (cobalt), Al (aluminum), Sn (tin), Ni (nickel), Mg (magnesium), and Ag (silver).

3.(Amended) The copper alloy for wiring as set forth in Claim 5, wherein

at the crystal grain boundaries and/or in the vicinities of grain boundaries, intermetallic compounds of Cu and at least one element selected from a group consisting of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag are formed.

4.(Amended) The copper alloy for wiring as set forth in Claim 5, wherein

at the crystal grain boundaries and/or in the vicinities of grain boundaries, oxides of at least one

element selected from a group consisting of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag are formed.

5.(Amended) A copper alloy for wiring composed of a polycrystalline copper alloy containing Cu (copper) as a primary element and an additional element, wherein

concentration of the additional element is, at grain boundaries of crystal grains composing the polycrystalline copper alloy and in vicinities of grain boundaries, higher than that of the inside of the crystal grains, and

concentration of the additional element in the crystal grains is 0.1 atomic percent or less.

6.(Amended) A semiconductor device comprising a substrate on which a semiconductor element is formed, and a metal wiring composed of the copper alloy for wiring as set forth in any one of Claims 1 through 5 and 17.

7. A method forming for a wiring comprising the steps of:

forming a polycrystalline Cu film;

forming, on the polycrystalline Cu film, a layer made of an additional element to be added into the Cu film; and

diffusing the additional element from the additional element layer into the polycrystalline Cu film.

8. The method for forming a wiring as set forth in Claim 7, wherein

a heating step of heating a substrate on which said polycrystalline Cu film has been formed, said step of forming the additional element layer, and said step of diffusing the additional element are simultaneously

performed.

9. The forming method for wiring as set forth in Claim 7 or 8, wherein

the additional element is at least one element selected from a group consisting of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

10. A method for manufacturing a semiconductor device comprising the steps of:

forming a polycrystalline Cu film on a substrate on which a semiconductor element is formed;

forming a layer composed of an additional element on the polycrystalline Cu film; and

diffusing the additional element from the additional element layer into the polycrystalline Cu film.

11. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a substrate on which a semiconductor element has been formed;

forming concavities for wiring composed of at least either grooves or holes in the insulating film;

forming a Cu film on the insulating film so as to fill up the concavities for wiring;

removing an excessive Cu film on the insulating film excluding parts buried in the concavities for wiring by chemical mechanical polishing;

forming a layer composed of an additional element on the Cu film;

diffusing the additional element from the additional

element layer into the Cu film; and

removing an excessive additional element layer.

12. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a substrate on which a semiconductor element has been formed;

forming concavities for wiring composed of at least either grooves or holes in the insulating film;

forming a barrier metal film to prevent Cu from diffusing on the surface of the insulating film including inner surfaces of the concavities for wiring;

forming a Cu film on the insulating film so as to fill up the same in the concavities for wiring;

removing a Cu film and a barrier metal film on the insulating film excluding parts buried in the concavities for wiring by chemical mechanical polishing;

forming a layer composed of an additional element on the Cu film in the concavities for wiring;

diffusing the additional element from the additional element layer into the Cu film; and

removing an excessive additional element layer.

13. The method for manufacturing a semiconductor device as set forth in Claim 11 or 12, wherein

said step of forming the additional element layer, said step of diffusing the additional element, and said step of removing the excessive additional element layer are performed before said step of removing the excessive Cu film.

14. The method for manufacturing a semiconductor

device as set forth in Claim 11 or 12, wherein

said step of forming the additional element layer, said step of diffusing the additional element, and said step of removing the excessive additional element layer are performed after said step of removing the excessive Cu film.

15. The method for manufacturing a semiconductor device as set forth in any one of Claims 10 through 14, wherein

a step of heating the substrate, said step of forming the additional element layer, and said step of diffusing the additional element are simultaneously performed.

16. The method for manufacturing a semiconductor device as set forth in any one of Claims 10 through 15, wherein

the additional element is at least one element selected from a group consisting of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

17.(Added) A copper alloy for wiring composed of a polycrystalline copper alloy containing Cu (copper) as a primary element and an additional element, wherein

concentration of the additional element is, at grain boundaries of crystal grains composing the polycrystalline copper alloy and in vicinities of grain boundaries, higher than that of the inside of the crystal grains, a barrier layer is formed to surround the polycrystalline copper alloy, and concentration of the additional element is, at the interface between the polycrystalline copper alloy and the barrier layer and in vicinities of said interface, higher

than that of the inside of the crystal grains.

WHAT IS CLAIMED IS:

1. A copper alloy for wiring composed of a polycrystalline copper alloy containing Cu (copper) as a primary element and an additional element, wherein

concentration of the additional element is, at grain boundaries of crystal grains composing the polycrystalline copper alloy and in vicinities of grain boundaries, higher than that of the inside of the crystal grains.

2. The copper alloy for wiring as set forth in Claim 1, wherein

the additional element is at least one element selected from a group consisting of Ti (titanium), Zr (zirconium), Hf (hafnium), Cr (chromium), Co (cobalt), Al (aluminum), Sn (tin), Ni (nickel), Mg (magnesium), and Ag (silver).

3. The copper alloy for wiring as set forth in Claim 2, wherein

at the crystal grain boundaries and/or in the vicinities of grain boundaries, intermetallic compounds of Cu and at least one element selected from a group consisting of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag are formed.

4. The copper alloy for wiring as set forth in Claim 2, wherein

at the crystal grain boundaries and/or in the vicinities of grain boundaries, oxides of at least one element selected from a group consisting of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag are formed.

5. The copper alloy for wiring as set forth in any

one of Claims 2 through 4, wherein

concentration of the additional element in the crystal grains is 0.1 atomic percent or less.

6. A semiconductor device comprising a substrate on which a semiconductor element is formed, and a metal wiring composed of the copper alloy for wiring as set forth in any one of Claims 1 through 5.

7. A method forming for a wiring comprising the steps of:

forming a polycrystalline Cu film;

forming, on the polycrystalline Cu film, a layer made of an additional element to be added into the Cu film; and

diffusing the additional element from the additional element layer into the polycrystalline Cu film.

8. The method for forming a wiring as set forth in Claim 7, wherein

a heating step of heating a substrate on which said polycrystalline Cu film has been formed, said step of forming the additional element layer, and said step of diffusing the additional element are simultaneously performed.

9. The forming method for wiring as set forth in Claim 7 or 8, wherein

the additional element is at least one element selected from a group consisting of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

10. A method for manufacturing a semiconductor device comprising the steps of:

forming a polycrystalline Cu film on a substrate on which a semiconductor element is formed;

forming a layer composed of an additional element on the polycrystalline Cu film; and

diffusing the additional element from the additional element layer into the polycrystalline Cu film.

11. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a substrate on which a semiconductor element has been formed;

forming concavities for wiring composed of at least either grooves or holes in the insulating film;

forming a Cu film on the insulating film so as to fill up the concavities for wiring;

removing an excessive Cu film on the insulating film excluding parts buried in the concavities for wiring by chemical mechanical polishing;

forming a layer composed of an additional element on the Cu film;

diffusing the additional element from the additional element layer into the Cu film; and

removing an excessive additional element layer.

12. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a substrate on which a semiconductor element has been formed;

forming concavities for wiring composed of at least either grooves or holes in the insulating film;

forming a barrier metal film to prevent Cu from diffusing on the surface of the insulating film including inner surfaces of the concavities for wiring;

forming a Cu film on the insulating film so as to fill up the same in the concavities for wiring;

removing a Cu film and a barrier metal film on the insulating film excluding parts buried in the concavities for wiring by chemical mechanical polishing;

forming a layer composed of an additional element on the Cu film in the concavities for wiring;

diffusing the additional element from the additional element layer into the Cu film; and

removing an excessive additional element layer.

13. The method for manufacturing a semiconductor device as set forth in Claim 11 or 12, wherein

said step of forming the additional element layer, said step of diffusing the additional element, and said step of removing the excessive additional element layer are performed before said step of removing the excessive Cu film.

14. The method for manufacturing a semiconductor device as set forth in Claim 11 or 12, wherein

said step of forming the additional element layer, said step of diffusing the additional element, and said step of removing the excessive additional element layer are performed after said step of removing the excessive Cu film.

15. The method for manufacturing a semiconductor device as set forth in any one of Claims 10 through 14, wherein

a step of heating the substrate, said step of forming the additional element layer, and said step of diffusing the additional element are simultaneously performed.

16. The method for manufacturing a semiconductor device as set forth in any one of Claims 10 through 15, wherein

the additional element is at least one element selected from a group consisting of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.